SEMICONDUCTOR DEVICE AND METHOD FOR MAKING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority of Taiwanese Application No. 092102324, filed on January 30, 2003.

BACKGROUND OF THE INVENTION

1. Field of the invention

This invention relates to a semiconductor device, and more particularly to a BGA-based (Ball Grid Array-based) semiconductor device and to a method for making the same.

2. Description of the related art

Conventional lead-based semiconductor devices normally include a semiconductor die with bonding pads that are connected electrically and respectively to leads of a lead frame through bonding wires so as to connect internal circuits of the semiconductor die to external circuits through the leads. The conventional semiconductor devices thus formed have relatively large dimensions. Conventional ball grid array (BGA)-based semiconductor devices have smaller dimensions as compared to those of the lead-based semiconductor devices. Assembly of different semiconductor dies in a single package is the current trend in the semiconductor industry for miniaturization of electronic devices. However, the conventional method for manufacturing a semiconductor die is normally inappropriate for a different one, which increases the difficulty for assembling different semiconductor dies in a single package and which may result in an increase in

manufacturing costs.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a semiconductor device that is capable of overcoming the aforesaid drawback of the prior art.

Another object of the present invention is to provide a method for making the semiconductor device.

According to one aspect of the present invention, there is provided a semiconductor device that comprises: a die-mounting substrate having a die-mounting surface and formed with a plurality of conductive contacts on the die-mounting surface; at least one semiconductor die attached to the die-mounting surface, having a pad-mounting surface opposite to the die-mounting surface, and formed with a plurality of spaced apart bonding pads on the pad-mounting surface; a dielectric interposer formed on the die-mounting surface and formed with at least one pad-through-hole and a plurality of contact-through-holes, the pad-through-hole receiving the die therein and exposing the pad-mounting surface therefrom, each of the contact-through-holes receiving a respective one of the contacts therein and exposing the respective one of the contacts therefrom; a plurality of conductive strips formed on the pad-mounting surface and the interposer, each of the conductive strips having a pad-connecting part

that is electrically connected to and that extends from a respective one of the bonding pads, and a trace part that extends from the pad-connecting part to connect electrically with a respective one of the conductive contacts; an encapsulant layer formed on the die-mounting surface, the interposer, the conductive strips, and the pad-mounting surface of the die, and formed with a plurality of bump-through-holes, each of which exposes a portion of the trace part of a respective one of the conductive strips therefrom; and a plurality of solder bumps, each of which fills a respective one of the bump-through-holes to connect electrically with the portion of the trace part of a respective one of the conductive strips and each of which protrudes outwardly from the encapsulant layer.

According to another aspect of the present invention, there is provided a method for making the semiconductor device. The method comprises the steps of: preparing a die-mounting substrate that has a die-mounting surface and that is formed with a plurality of conductive contacts on the die-mounting surface; preparing a semiconductor die that has a pad-mounting surface, and a plurality of spaced apart bonding pads formed on the pad-mounting surface; attaching the semiconductor die to the die-mounting surface; preparing a dielectric interposer that is

formed with a pad-through-hole and a plurality of contact-through-holes; attaching the interposer to the die-mounting surface in such a manner that the die is received in and is exposed from the pad-through-hole and that each of the contacts is received in and is exposed from a respective one of the contact-through-holes; forming a plurality of conductive strips on the pad-mounting surface and the interposer, each of the conductive strips having a pad-connecting part that is electrically connected to and that extends from a respective one of the bonding pads, and a trace part that extends from the pad-connecting part to connect electrically with a respective one of the conductive contacts; forming an encapsulant layer on the die-mounting surface, the interposer, and the conductive strips; forming a plurality of bump-through-holes in the encapsulant layer in such a manner that each of the bump-through-holes exposes a portion of the trace part of a respective one of the conductive strips; and forming a plurality of solder bumps, each of which fills a respective one of the bump-through-holes to connect electrically with the portion of the trace part of a respective one of the conductive strips, and each of which protrudes outwardly from the protective layer.

BRIEF DESCRIPTION OF THE DRAWINGS

In drawings which illustrate embodiments of the invention,

Fig. 1 is a schematic view to illustrate how a semiconductor die is attached to a die-mounting substrate for forming a semiconductor device according to the first preferred embodiment of a method of this invention;

Fig. 2 is a schematic view to illustrate how a dielectric interposer is provided on the die-mounting substrate according to the first preferred embodiment of this invention;

Fig. 3 is a schematic view to illustrate how a conductive strip is formed on the die and the interposer according to the first preferred embodiment of this invention;

Fig. 4 is a schematic view to illustrate how an encapsulant layer is formed on the assembly of Fig. 3 according to the first preferred embodiment of this invention;

Fig. 5 is a schematic view to illustrate how a solder bump is formed on the encapsulant layer and is electrically connected to the conductive strip according to the first preferred embodiment of this invention;

Fig. 6 is a schematic view showing a modified semiconductor device that is modified from that shown

in Fig. 5;

Fig. 7 is a schematic view to illustrate how a dielectric interposer is formed on a die-mounting substrate for forming a semiconductor device according to the second preferred embodiment of the method of this invention;

Fig. 8 is a schematic view to illustrate how a semiconductor die is mounted in a through-hole in the interposer of Fig. 7 according to the second preferred embodiment of this invention;

Fig. 9 is a schematic view to illustrate how a conductive strip is formed on the die and the interposer of Fig. 8 according to the second preferred embodiment of this invention;

Fig. 10 is a schematic view to illustrate how an encapsulant layer is formed on the assembly of Fig. 9 according to the second preferred embodiment of this invention;

Fig. 11 is a schematic view to illustrate how a solder bump is formed on the encapsulant and is electrically connected to the conductive strip according to the second preferred embodiment of this invention;

Fig. 12 is a schematic perspective view of the semiconductor device formed according to the second preferred embodiment of this invention, with the encapsulant layer removed for the sake of clarity;

Fig. 13 is a perspective view of the semiconductor device formed according to the second preferred embodiment of this invention;

Fig. 14 is a schematic view to illustrate how a die-mounting recess is formed in a die-mounting substrate for forming a semiconductor device according to the third preferred embodiment of this invention;

Fig. 15 is a schematic view to illustrate how a semiconductor die is mounted in the die-mounting recess according to the third preferred embodiment of this invention;

Fig. 16 is a schematic view to illustrate how conductive strips are formed on the die-mounting substrate and the semiconductor die according to the third preferred embodiment of this invention;

Fig. 17 is a schematic view to illustrate how an encapsulant layer is formed on the assembly of Fig. 16 according to the third preferred embodiment of this invention;

Fig. 18 is a schematic view to illustrate how solder bumps are formed on the encapsulant layer and are electrically and respectively connected to the conductive strips according to the third preferred embodiment of this invention;

Fig. 19 is a perspective view of the semiconductor device formed according to the third

preferred embodiment of this invention, with the encapsulant layer removed for the sake of clarity;

Fig. 20 is a schematic perspective view of the semiconductor device formed according to the third preferred embodiment of this invention;

Fig. 21 is a schematic view to illustrate how a first conductive strip is formed on a die-mounting substrate for forming a semiconductor device according to the fourth preferred embodiment of this invention;

Fig. 22 is a schematic view to illustrate how a semiconductor die is attached to a die-mounting substrate according to the fourth preferred embodiment of this invention;

Fig. 23 is a schematic view to illustrate how a second conductive strip is formed on the die and the first conductive strip according to the fourth preferred embodiment of this invention;

Fig. 24 is a schematic view to illustrate how an encapsulant is formed on the assembly of Fig. 23 according to the fourth preferred embodiment of this invention;

Fig. 25 is a schematic view to illustrate how first and second solder bumps are formed on the encapsulant and are electrically and respectively connected to the first and second conductive strips according to the fourth preferred embodiment of this

invention;

Fig. 26 is a schematic view to illustrate how a first semiconductor die is attached to a die-mounting substrate for forming a semiconductor device according to the fifth preferred embodiment of a method of this invention;

Fig. 27 is a schematic view to illustrate how a dielectric interposer is provided on the die-mounting substrate according to the fifth preferred embodiment of this invention;

Fig. 28 is a schematic view to illustrate how a first conductive strip is formed on the first semiconductor die and the interposer according to the fifth preferred embodiment of this invention;

Fig. 29 is a schematic view to illustrate how a first encapsulant layer is formed on the assembly of Fig. 28 according to the fifth preferred embodiment of this invention;

Fig. 30 is a schematic view to illustrate how a second semiconductor die is attached to the first encapsulant layer according to the fifth preferred embodiment of this invention;

Fig. 31 is a schematic view to illustrate how a second conductive strip is formed on the second semiconductor die and is electrically connected to the first conductive strip according to the fifth preferred embodiment of this invention;

Fig. 32 is a schematic view to illustrate how a second encapsulant layer is formed on the assembly of Fig. 31 according to the fifth preferred embodiment of this invention;

Fig. 33 is a schematic view to illustrate how a solder bump is formed on the second encapsulant layer and is electrically connected to the second conductive strip according to the fifth preferred embodiment of this invention;

Fig. 34 is a schematic view to illustrate how a first conductive strip is formed on a semiconductor die for forming a semiconductor device according to the sixth preferred embodiment of this invention;

Fig. 35 is a schematic view to illustrate how a first encapsulant layer is formed on the first conductive strip and the semiconductor die to form a semi-package according to the sixth preferred embodiment of this invention;

Fig. 36 is a schematic view to illustrate how the semi-package is attached to a die-mounting substrate according to the sixth preferred embodiment of this invention;

Fig. 37 is a schematic view to illustrate how an interposer is formed on the semi-package according to the sixth preferred embodiment of this invention;

Fig. 38 is a schematic view to illustrate how a second conductive strip is formed on the interposer

according to the sixth preferred embodiment of this invention;

Fig. 39 is a schematic view to illustrate how a second encapsulant layer is formed on the assembly of Fig. 38 and how a solder bump is formed on the second encapsulant layer and is electrically connected to the second conductive strip according to the sixth preferred embodiment of this invention;

Fig. 40 is a perspective view to illustrate a semiconductor device formed according to the second preferred embodiment, with the encapsulant layer removed for the sake of clarity;

Fig. 41 is a perspective view to illustrate a memory device formed according to the second preferred embodiment, with the encapsulant layer removed for the sake of clarity; and

Fig. 42 is a schematic perspective view to illustrate a flash memory device formed according to the second preferred embodiment, with the encapsulant layer being removed.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

For the sake of brevity, like elements are denoted by the same reference numerals throughout the disclosure.

Figs. 1 to 5 illustrate consecutive steps of forming a semiconductor device according to the first preferred embodiment of the method of this invention.

The method of this embodiment includes the steps of: preparing a die-mounting substrate 1 that has a die-mounting surface 10 and that is formed with a plurality of conductive contacts 11 on the die-mounting surface 10 (see Fig. 1) and a plurality of traces connected to the contacts 11, respectively; preparing a semiconductor die 2 that has a pad-mounting surface 20, and a plurality of spaced apart bonding pads 21 formed on the pad-mounting surface 20 (only one is shown), each of the bonding pads 21 being preferably formed with a metal plating layer (not shown); attaching the semiconductor die 2 to the die-mounting surface 10 (see Fig. 1); preparing a dielectric interposer 3, such as a resinous packaging substrate, that is formed with a pad-through-hole 31 and a plurality of contact-through-holes 30 (see Fig. 2); attaching the interposer 3 to the die-mounting surface 10 in such a manner that the die 2 is received in the pad-through-hole 31 and has the pad-mounting surface 20 thereof exposed from the pad-through-hole 31 and that each of the contacts 11 is registered with and is exposed from a respective one of the contact-through-holes 30 (see Fig. 2); forming a plurality of conductive strips 4 on the pad-mounting surface 20 and the interposer 3 (see Fig. 3), each of the conductive strips 4 having a pad-connecting part 41 that is electrically connected to and that

extends from a respective one of the bonding pads 21, and a trace part 42 that extends from the pad-connecting part 41 to connect electrically with a respective one of the conductive contacts 11, each of the conductive strips 4 being made from a conductive paste; forming an encapsulant layer 5 on the die-mounting surface 10, the pad-mounting surface 20, the interposer 3, and the conductive strips 4 (see Fig. 4); forming a plurality of bump-through-holes 50 in the encapsulant layer 5 in such a manner that each of the bump-through-holes 50 exposes a portion of the trace part 42 of a respective one of the conductive strips 4; and forming a plurality of solder bumps 6, each of which fills a respective one of the bump-through-holes 50 to connect electrically with the exposed portion of the trace part 42 of a respective one of the conductive strips, and each of which protrudes outwardly from the encapsulant layer 5. Note that the trace part 42 of each conductive body 4 preferably has a metal layer 40 (see Fig. 3), which is electrically connected to the respective solder bump 6 and which includes a nickel sub-layer 401 and a gold sub-layer 402 so as to increase the conductivity of the conductive strips 4. The die-mounting substrate 1 is preferably a printed circuit board, or is made from a material selected from a group consisting of polyimide, glass, and ceramic. The

encapsulant layer 5 is preferably made from polyimide or photo ink.

Fig. 6 illustrates a modified semiconductor device formed according to the first embodiment of this invention. The modified semiconductor device includes two semiconductor dies 2 on a die-mounting substrate 1.

Figs. 7 to 11 illustrate consecutive steps of forming a semiconductor device according to the second preferred embodiment of the method of this invention. Unlike the previous embodiment, the interposer 3, which is preferably made from photo ink or polyimide, is formed on the die-mounting substrate 1 prior to the attachment of the semiconductor die 2 to the die-mounting substrate 1 (see Fig. 7), and is patterned and etched to form the pad-through-hole 31 for receiving the semiconductor die 2 therein (see Fig. 8), and the contact-through-holes 30. Subsequent steps of formation of the conductive strips 4, the encapsulant layer 5, and the solder bumps 6 (see Figs. 9 to 11) are similar to those of the previous embodiment.

Figs. 12 and 13 are perspective views to illustrate the semiconductor device formed according to the second preferred embodiment of the method of this invention. Fig. 12 shows the semiconductor device with the encapsulant layer 5 removed for the

sake of clarity. Fig. 13 shows the semiconductor device with the encapsulant layer 5. Two of the semiconductor dies 2 are built into the semiconductor device.

Figs. 14 to 18 illustrate consecutive steps of forming a semiconductor device according to the third preferred embodiment of the method of this invention.

Unlike the first preferred embodiment, the die-mounting substrate 1 is formed with a die-mounting recess 12 for receiving the semiconductor die 2, such as a CPU or a chip set therein, (see Figs. 14 and 15). The interposer 3 is eliminated in this embodiment. Subsequent steps of formation of the conductive strips 4, the encapsulant layer 5, and the solder bumps 6 (see Figs. 16 to 18) are similar to those of the first embodiment.

Figs. 19 and 20 illustrate the semiconductor device formed according to the third preferred embodiment. Fig. 19 shows the semiconductor device with the encapsulant layer 5 removed. Fig. 20 shows the semiconductor device with the encapsulant layer 5 and the solder bumps 6

Figs. 21 to 25 illustrate consecutive steps of forming a semiconductor device according to the fourth preferred embodiment of the method of this invention. The method of this embodiment includes the steps of: preparing a die-mounting substrate 1 that

has a die-mounting surface 10 and that is formed with a plurality of conductive contacts 11 on the die-mounting surface 10 (see Fig. 21); forming a plurality of first conductive strips 4 on the die-mounting surface 10 (see Fig. 22), each of the first conductive strips 4 being electrically connected to and extending from a respective one of the contacts 11 in a lateral direction relative to the die-mounting surface 10; preparing a semiconductor die 2 that has a pad-mounting surface 20, and that is formed with a plurality of spaced apart bonding pads 21 on the pad-mounting surface 20 (see Fig. 22); attaching the semiconductor die 2 to the die-mounting surface 10; forming a plurality of second conductive strips 4' (see Fig. 23), each of which is formed on the pad-mounting surface 20 and each of which is electrically connected to and extends from a respective one of the bonding pads 21 in the lateral direction to connect electrically with a first portion 41 of a respective one of the first conductive strips 4; forming an encapsulant layer 5 on the die-mounting surface 10, the first and second conductive strips 4, 4', and the pad-mounting surface 20 of the die 2 (see Fig. 24); patterning and etching the encapsulant layer 5 to form a plurality of first and second bump-through-holes 50, 50' in the encapsulant layer 5 in such a manner that each of the

first bump-through-holes 50 exposes a second portion 42 of a respective one of the first conductive strips 4 therefrom, and that each of the second bump-through-holes 50' exposes a portion of a respective one of the second conductive strips 4' therefrom, the first and second portions 41, 42 of each of the first conductive strips 4 being offset from each other in the lateral direction (see Fig. 24); and forming a plurality of first and second solder bumps 6, 6' (see Fig. 25) in such a manner that each of the first solder bumps 6 fills a respective one of the first bump-through-holes 50 to connect electrically with the second portion 42 of a respective one of the first conductive strips 4 and protrudes outwardly from the encapsulant layer 5, and that each of the second solder bumps 6' fills a respective one of the second bump-through-holes 50' to connect electrically with the exposed portion of a respective one of the second conductive strips 4' and protrudes outwardly from the encapsulant layer 5. Each of the first and second conductive strips 4, 4' includes a metal layer 40 that is electrically connected to a respective one of the first and second solder bumps 6, 6'. Each metal layer 40 includes a nickel sub-layer 401 and a gold sub-layer 402 (see Fig. 22).

Figs. 26 to 33 illustrate consecutive steps of forming a semiconductor device according to the fifth

preferred embodiment of the method of this invention. Figs. 26 to 30 illustrate steps that are similar to those of Figs. 1 to 4. However, unlike the first preferred embodiment, a second semiconductor die 2' is attached to the encapsulant layer 5 (see Fig. 30), and a plurality of second conductive strips 4' (see Fig. 31) and a second encapsulant layer 5' (see Fig. 32) are subsequently formed on the encapsulant layer 5 prior to the formation of the solder bumps 6 (see Fig. 33). The encapsulant layer 5 is formed with a plurality of strip-through-holes 50, each of which exposes a portion of the trace part 42 of a respective one of the first conductive strips 4 therefrom (see Fig. 30). Each of the second conductive strips 4' is formed on the first encapsulant layer 5, is electrically connected to a respective one of the bonding pads 21' of the second semiconductor die 2', and fills a respective one of the strip-through-holes 50 to connect electrically with the exposed portion of the trace part 42 of a respective one of the first conductive strips 4 (see Fig. 31). The second encapsulant layer 5' is formed on the first encapsulant layer 5, the second semiconductor die 2', and the second conductor strips 4', and is patterned and etched to form a plurality of bump-through-holes 50' in the second encapsulant layer 5' in such a manner that each of the bump-through-holes 50' exposes a

portion of a respective one of the second conductive strips 4' (see Fig. 32). Each of the solder bumps 6 fills a respective one of the bump-through-holes 50' to connect electrically with a respective one of the second conductive strips 4'.

Figs. 34 to 39 illustrate consecutive steps of forming a semiconductor device according to the sixth preferred embodiment of the method of this invention. The method of this embodiment includes preparation of a die-mounting substrate 1 that has a die-mounting surface 10 and that is formed with a plurality of conductive contacts 11 on the die-mounting surface 10 (see Fig. 36). A semiconductor semi-package 100 is prepared by the following steps: preparing a semiconductor die 2 that has a pad-mounting surface 20, and that is formed with a plurality of spaced apart bonding pads 21 on the pad-mounting surface 20 (see Fig. 34); forming a plurality of first conductive strips 4, each of which is formed on the pad-mounting surface 20 and each of which is electrically connected to and extends from a respective one of the bonding pads 21 in a lateral direction relative to the pad-mounting surface 20 (see Fig. 34); forming a first encapsulant layer 5 on the pad-mounting surface 20 and the first conductive strips 4; and patterning and etching the first encapsulant layer 5 to form a plurality of strip-through-holes 50 in the first

encapsulant layer 5 in such a manner that each of the strip-through-holes 50 exposes a portion of a respective one of the first conductive strips 4 therefrom. The method further includes the steps of: attaching the semi-package 100 to the die-mounting surface 10 (see Fig. 36); forming a dielectric interposer 3 with a die-through-hole 31 and a plurality of contact-through-holes 30 on the die-mounting surface 10 in such a manner that the die-through-hole 31 receives the semi-package 100 therein and exposes the semi-package 100 therefrom, and that each of the contact-through-holes 30 is registered with a respective one of the contacts 11 and exposes the respective one of the contacts 11 therefrom, the interposer 3 being in the form of a resin packaging substrate; forming a plurality of second conductive strips 4' on the interposer 3 and the semi-package 100 in such a manner that each of the second conductive strips 4' has a first portion 41' that fills a respective one of the strip-through-holes 50 in the first encapsulant layer 5 to connect electrically with the exposed portion of a respective one of the first conductive strips 4, and a second portion 42' that fills a respective one of the contact-through-holes 30 to connect electrically with a respective one of the contacts 11; forming a second encapsulant layer 5' on the interposer 3, the

second conductive strips 4', and the semi-package 100; patterning and etching the second encapsulant layer 5' to form a plurality of bump-through-holes 50' in the second encapsulant layer 5' in such a manner that each of the bump-through-holes 50' exposes a third portion 43' of a respective one of the second conductive strips 4' therefrom; and forming a plurality of solder bumps 6, each of which fills a respective one of the bump-through-holes 50' to connect electrically with the third portion 43' of a respective one of the second conductive strips 4' and each of which protrudes outwardly from the second encapsulant layer 5'. Similar to the previous embodiments, each of the first and second conductive strips 4, 4' includes a metal layer 40 that has a nickel sub-layer 401 and a gold sub-layer 402.

Fig. 40 shows a semiconductor device with the encapsulant layer 5 removed to illustrate an inner structure thereof. The device includes a plurality of semiconductor dies 2 attached to a die-mounting substrate 1.

Fig. 41 shows a memory device with the encapsulant layer 5 removed to illustrate an inner structure thereof. The device includes a plurality of semiconductor dies 2 attached to a die-mounting substrate 1.

Fig. 42 shows a flash memory device with the

encapsulant layer 5 removed to illustrate an inner structure thereof. The device includes a plurality of memory dies 2 and a controller die 2' attached to a die-mounting substrate 1.

Figs. 43 to 46 illustrate consecutive steps of forming a semiconductor device according to the seventh preferred embodiment of the method of this invention. Unlike the first embodiment, the interposer 3, which is preferably made from photo ink or polyimide, is formed on the die-mounting substrate 1 (which is a glass back plate for a display panel) prior to the attachment of the semiconductor die 2 to the die-mounting substrate 1 (see Fig. 43), and is patterned and etched to form the pad-through-hole 31 for receiving the semiconductor die 2 therein (see Fig. 44), and the contact-through-holes 30 for exposing the contacts 11 (which are electrically connected to the display panel) on the die-mounting surface 10. A plurality of conductive strips 4 (only one is shown) are formed on the interposer 3 (see Fig. 45), and are connected to the bonding pads 21, respectively. Each of the conductive strips 4 extends from the respective bonding pads 21 to a respective one of the contact-through-holes 30, and fills the respective one of the contact-through-holes 30 to connect electrically a respective one of the contacts 11. Each of the conductive strips 4 is formed with

a metal layer 40. An encapsulant layer 5 is subsequently formed on the interposer 3 and the conductive strips 4 (see Fig. 46).

With the invention thus explained, it is apparent that various modifications and variations can be made without departing from the spirit of the present invention. It is therefore intended that the invention be limited only as recited in the appended claims.